UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,939	08/26/2003	John L. Galvagni	AVX-187-DIV	3080

22827 7590 01/04/2007

DORITY & MANNING, P.A.
POST OFFICE BOX 1449
GREENVILLE, SC 29602-1449

EXAMINER	
PHAN, THIEM D	
ART UNIT	**PAPER NUMBER**
3729	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

NT

Office Action Summary	Application No.	Applicant(s)	
	10/647,939	GALVAGNI ET AL.	
	Examiner	Art Unit	
	Tim Phan	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 12/07/06 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 6, 7, 10 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Novak (US 6,215,372).

With regard to claim 6, Novak teaches a method for reducing electrical resonances and noise propagation in multilayer board, comprising:

- producing a multilayer component (Fig. 6, 600) including at least first and second electrically conductive layers (Fig. 6, items 602 and 606) separated by an insulating layer (Fig. 6, item 610);
- providing a resistive layer (Fig. 6, 650 or 652; col. 9, lines 6-12) with the insulating layer and the first and second electrically conductive layers; and

- adjusting the ESR (Col. 8, lines 59-61; col. 9, lines 5-20) of the component by varying the effective resistance of the resistive layer.

With regard to claim 7, Novak teaches that the providing step comprises:

- providing the resistive layer (Fig. 6, 650 or 652) between the insulating layer (Fig. 6, 610) and one of the first or second electrically conductive layers (Fig. 6, 606).

With regard to claims 10 and 12, Novak teaches that the adjusting step comprises:

- varying the effective resistance of the resistive layer by adjusting the composition of the resistive layer (Col. 9, lines 5-20).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8, 9, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Novak.

With regard to claim 8, Novak teaches a method for reducing electrical resonances and noise propagation in multilayer board, including the adjusting steps of:

- perforating one of the first or second electrically conductive layers (Fig. 6, items 602 or 606; Fig. 10, items 1002 or 1006) with a plurality of through-holes (Fig. 6, 622; Fig. 10,

1022); and

- varying the effective resistance of the resistive layer by adjusting capacitive and resistive islands (Fig. 6, 652 or Fig. 10, 1052; col. 9, lines 6-29) at selected areas or distances (Fig. 6, See Below; col. 9, lines 37-49) from vias (Fig. 6, 622 or Fig. 10,1022) whereby the extent of coverage of the perforated electrode varies the effective resistance of the resistive layer, except for detailing these selected areas or distances as varying and spacing diameters of through-holes.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to consider these selected areas or distances as varying and spacing diameters (Fig. 6, See Below; col. 9, lines 37-49) of through-holes, which can vary to adjust the resistance/ capacitance and to match the impedance of the multilayer circuit in order to reduce noise and any ground bounced signal in the whole printed circuit board.

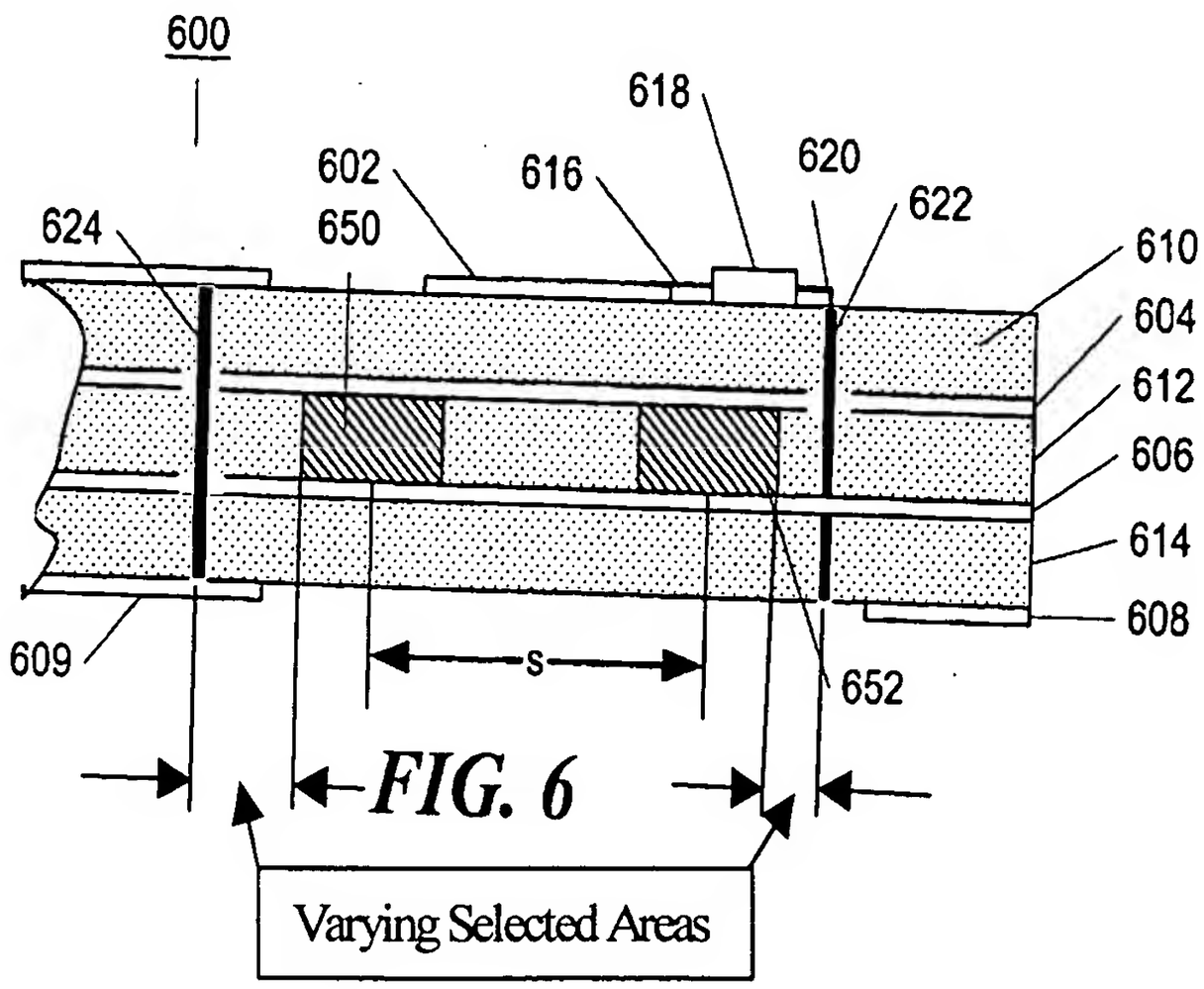


FIG. 6

With regard to claims 9 and 11, Novak teaches that the adjusting step comprises the adjustment of the ESR (Col. 8, lines 59-61; col. 9, lines 5-20) of the multilayer component by varying the effective resistance of the resistive layer (Fig. 6, 652) through changing its resistive material, which reads on applicants' claimed invention.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to realize that a further adjustment of the thickness of the resistive layer (Fig. 6, 652) will further vary the effective resistance of the resistive layer as the resistance or impedance of a device is dependent on its thickness or size.

With regard to claim 13, Novak teaches a method for reducing electrical resonances and noise propagation in multilayer board, which reads on applicants' claimed invention, including:

- producing a multilayer component (Fig. 6, 600) having a plurality of successively stacked electrode layers (Fig. 6, items 602, 604, 606 or 608);
- providing separate insulating layers (Fig. 6, items 610, 606 or 614) sandwiched between each of the electrode layer; and
- varying a physical property of the selected, separated, insulating layers with different capacitance (Fig. 6, 652) whereby the resonance characteristics of the multi-layer component are adjusted (Abstract); except for having two separate insulating layers characterized by two different thicknesses, whereby the resonance characteristics of the multi-layer component are adjusted.

It is mere matter of design choice to have two separate insulating layers characterized by

two different thicknesses or more or less, whereby the resonance characteristics of the multi-layer component are adjusted, since it is known in the art that the physical property or capacitance is dependent also on the thickness (Fig. 1, h) and the dielectric constant (epsilon-r) of the insulating layer based on the mentioned equation in column 8, lines 41-44, therefore one of ordinary skill in the art, by applying the mentioned equation (Col. 5, line 10), can vary the capacitance of the conductors (Fig. 10, items 1002, 1004, 1006 or 1008) or the overall multi-layer component by varying the dielectric constant (Fig. 10, 1052; col. 7, lines 43-48) and/or the thickness of the insulating layers (Fig. 10, items 1010 or 1012 or 1014) of the substrate in order to come up with the desired capacitance for the conductors on that substrate for proper resonance. Therefore, varying some of the insulating layers' thickness (Fig. 10, 1010 or 1012) or the dielectric constant of the component (Fig. 10, 1052; col. 9, lines 6-9) will provide the same effect of varying the capacitance of the conductors, which results in adjusting the resonance characteristics of the multi-layer component.

Response to Arguments

6. Applicants' arguments filed 12/07/06 have been fully considered but they are not persuasive for the following reasons:

Applicant's arguments with respect to claim 6 (Remarks; pages 10 & 11) fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the reference.

Applicants' assertions that the islands 650 or 652, as taught by the prior art Novak, are not resistive layer and not separable from other layers (Remarks, page 12) are traversed since Novak teaches that the dielectric islands can have its adjusting resistance by suspending conductive particles within its binder material (Col. 9, lines 6-9) and separate from different layers (Fig. 6, items 602, 610, 604, 606, 614 or 608). Therefore, his islands are completely associated with the capacitance and resistance characteristics, which are critical part in matching signal impedance in order to reduce resonance in any circuit system.

With respect to applicants' citations in page 13, it appears that applicants try to miscompare the prior art Novak and the claimed invention. Applicants are invited to revisit the claimed rejection as stated in section 3 above.

Regarding the arguments (Pages 14-17) about the remainder of the claims, i.e. Claims 7-13, these claims stand rejected with the reasoning for their rejections as carefully articulated in the previous or newly processed in the instant Office Action and in view of the responses in the paragraphs above.

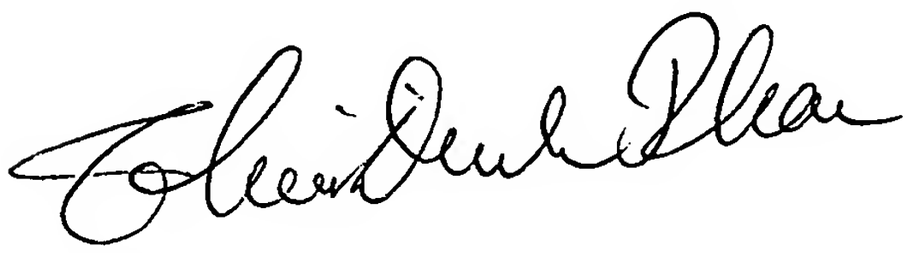
Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M & Tu, 6AM - 2PM, and W & Th, 9AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tim Phan
Examiner
Art Unit 3729

tp
December 26, 2006